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06CS33

Third Semester B.E. Degree Examination, June/July 2011

Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions selecting at least TWO questions from each part.***

PART – A

1 a. Explain the significance of DeMorgan's theorem. **(04 Marks)**

b. Simplify the following function using k-map and design it by using NAND gates (use only four gates):

$f = w'xz + w'yz + x'yz' + wxy'z$; $d = wyz$ **(08 Marks)**

c. Define prime implicant and essential prime implicant. Find prime implicant and essential prime implicantor for the following function using Quine-Mcclusky method :

$f(a,b,c,d) = \sum m(0,2,3,6,7,8,10,12,13)$ **(08 Marks)**

2 a. What is multiplexer? Design 4 : 1 multiplexer and implement using gates. **(04 Marks)**

b. Implement the following function using decoder :

$F_1(A,B,C) = \sum m(0,4,6)$; $F_2(A,B,C) = \sum m(0,5)$; $F_3(A,B,C) = \sum m(1,2,3,7)$. **(08 Marks)**

c. Implement the following function using PLA :

$X = A'B'C + AB'C' + B'C$; $Y = A'B'C + AB'C'$; $Z = B'C$. **(08 Marks)**

3 a. i) Convert the following decimal numbers into their binary equivalent :

A) 10 B) 15 C) 2 D) 4

ii) Represent all the above numbers as :

A) Unsigned binary numbers B) Sign magnitude numbers

C) 1's complement of each number D) 2's complement of each number

iii) Illustrate the following operators:

A) +67, –98 (8 bit binary addition) B) +16, –38 (8 bit binary subtraction)

(08 Marks)

b. Explain the working principle of 2-bit fast adder with neat diagram. **(08 Marks)**

c. Write HDL design of full adder. **(04 Marks)**

4 a. Draw the state transition of the circuit shown in Fig.Q4(a) : **(06 Marks)**

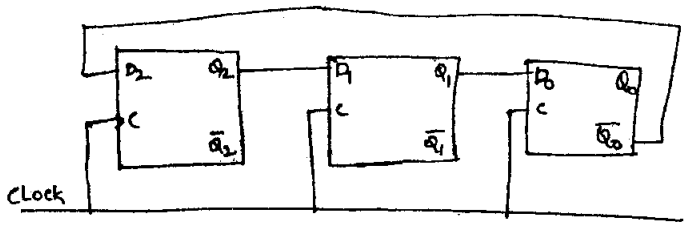

Fig.Q4(a)

b. With the help of neat diagram explain the working of Master-Slave JK Flip Flop. Mention its advantages. **(10 Marks)**

c. Write HDL design of D-Flip Flop. **(04 Marks)**

PART – B

5 a. Design a mod-6 synchronous upcounter using JK-Flip-Flop. **(08 Marks)**

b. Define shift register? Explain 4-bit switched tail counter with neat diagram. **(08 Marks)**

c. Design 3-bit ripple counter. **(04 Marks)**

6 a. Design a sequence detector that receives binary data stream at its input X and signals when a combination "1011" arrives at the input by masking its output Y high which otherwise remains low. Consider data is coming from left, that is, the first bit to be identified is 1, second is 1, third is 0 from input sequence. **(06 Marks)**

b. Differentiate between Mealy machine and Moore machines. **(04 Marks)**

c. Reduce state diagram shown in Fig.Q6(c) (Moore model) using following methods:
i) Row elimination method ii) Implication table method **(10 Marks)**

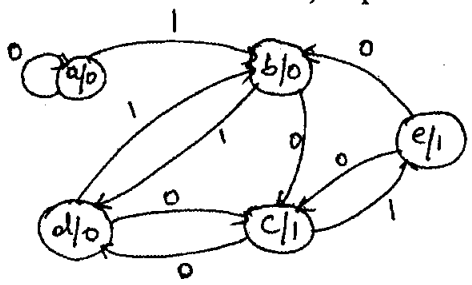

Fig.Q6(c)

7 a. Explain A/D converter by using counter method. **(08 Marks)**

b. Explain the following with neat diagram :
i) TTL NOR ii) 2-input CMOS NOR
iii) TTL NAND iv) 2-input CMOS NAND **(12 Marks)**

8 a. With the help of the circuit diagram explain the working of a 4-bit D/A converter. **(08 Marks)**

b. Write short notes on: **(12 Marks)**
i) Magnitude comparator
ii) CMOS characteristics
iii) Racing
iv) Totem pole.

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